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Modified single-switch bridgeless PFC SEPIC structure by eliminating circulating current and power quality improvement

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Abstract: In this study, a modified single-switch bridgeless power factor correction (PFC) single-ended primary-inductor converter (SEPIC) structure is proposed. The major practical drawbacks of the existing structure are the presence of circulating current and high maximum current stress at the input capacitor and line diodes. Therefore, to overcome these problems, the existing structure is restructured by repositioning the line diodes in series with input inductors. Besides, the principle of design parameters optimisation is used based on the balancing energy compensation between input capacitors and output inductor. This structure is designed to operate in discontinuous conduction mode in order to achieve almost a unity power factor. The operation principle and design consideration of the modified structure is introduced in details. The experimental results demonstrate that the total harmonic distortion current is reduced from 56.3 to 4.9% after the optimisation process is performed, and at the same time the dead zones are inherently eliminated. Furthermore, it is shown that the output voltage ripple frequency is always double from the input line frequency of 50 Hz and the output voltage ripple is constantly lower than the maximum input voltage ripple. Thus, the designed parameters of the experimental converter are verified with ∼160 W of the converter output power.

1 Introduction

Portable electronic equipment has advanced from power converter and has the advantages of high efficiency, small in size, and possesses a wide input and output voltage ranges [1–3]. On the other hand, the conventional power converter is not able to operate in a wide operation range and at the same time maintaining a high efficiency; especially, when the stepped-up and stepped-down voltage conversion need to be achieved [2, 4, 5]. In addition, voltages of the battery decrease as the battery discharges and leads to various difficulties if there is no voltage control function [6]. The most effective method of regulating the voltages through a circuit is by using a DC–DC converter. Hence, a SEPIC structure can be used as a DC voltage regulator due to the ability of the converter to step-up or step-down the voltages as shown in Fig. 1. For example, a 48 V nominal output voltage from a single input voltage source is useful in various cases such as electrical machines, light-emitting diode applications, solar energy systems, electric vehicle, data communication, and telecommunication power systems [7–11].

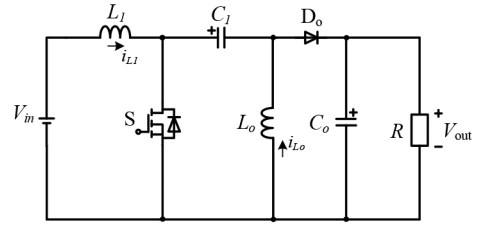

Fig. 1 *SEPIC structure*

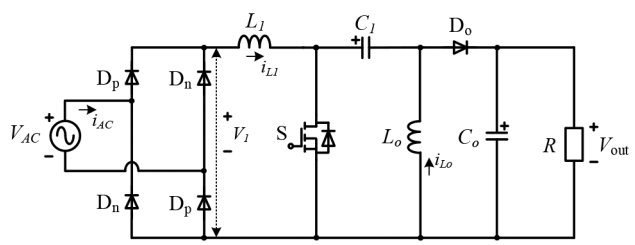

Fig. 2 *Conventional PFC SEPIC structure*

Some power application systems require an AC supply as the input source. Meanwhile, rectifiers and DC–DC converters are used to convert AC–DC according to the load requirements. Nevertheless, the use of bridge rectifier, transformer, inductor, and capacitor can produce a DC output voltage without distortion but will cause the input current to be extremely distorted. Hence, AC–DC conversion is immensely required in PFC converters to ensure the waveform of input voltage and input current sources are purely sinusoidal without the occurrence of dead zones [12, 13]. The dead zones occur when the output full bridge V_1 contains extra energy caused by the energy imbalance between input capacitor C_1 and output inductor L_o, which leads to the deterioration of sinusoidal input current and power factor (PF). Several circuit topologies such as boost, buck–boost, SEPIC, and Cuk converters have been developed for PFC applications [14–18].

The conventional PFC SEPIC structure consists of full-bridge rectifier and SEPIC, as shown in Fig. 2. It is common for the circuit structure to face power quality issues when the two structures are integrated. For instance, high-current total harmonic distortion (THD) (THD_i), low PF, dead zones, and high-output voltage ripple [19–21]. The output voltage from the full-bridge rectifier (V_1) is not a constant DC voltage. Therefore, the energy from the V_1 must be transferred to the SEPIC effectively without incurring any additional energy. If the energy is not effectively transferred, the THD_i at the input sources might be affected which increases the output voltage ripple [22]. Thus, the conventional bridgeless PFC SEPIC structure as in [23, 24] which can be viewed

in Fig. 3 is introduced to overcome the drawbacks of the conventional PFC SEPIC structure.

Moreover, the conventional bridgeless consists of two switches, where the control of the circuit is even more complex [25–27]. Besides, the input voltage and current sources are not in-phase, which will eventually deteriorate the PF of conventional bridgeless. Nevertheless, the advantage of the conventional bridgeless is it only requires one diode rectifier to conduct during positive-half and negative-half cycles [28].

The existing single-switch bridgeless PFC SEPIC structure [29] has been introduced to reduce the number of switches and increase the PF, as shown in Fig. 4. This structure allows the AC voltage and current sources to be in-phase. However, this structure suffers from major practical drawbacks that foresee the need to be considered which are circulating current at the input inductors (L_1 and L_2) and also the maximum current stress at line diodes (D_1 and D_2) and input capacitors (C_1 and C_2). The circulating current occurs due to the positions of D_1 and D_2, which are connected to

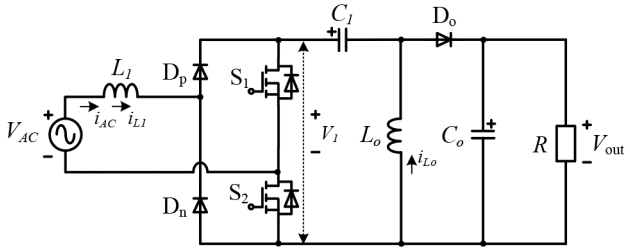

Fig. 3 *Conventional bridgeless PFC SEPIC structure [23, 24]*

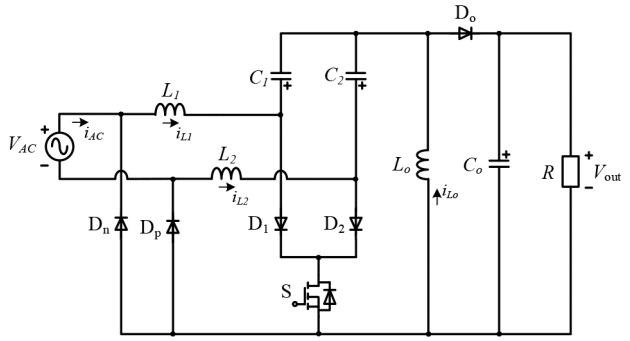

Fig. 4 *Existing single-switch bridgeless PFC SEPIC converter structure [29]*

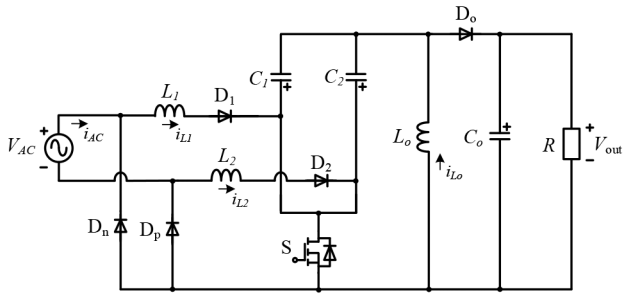

Fig. 5 *Proposed modified single-switch bridgeless PFC SEPIC structure*

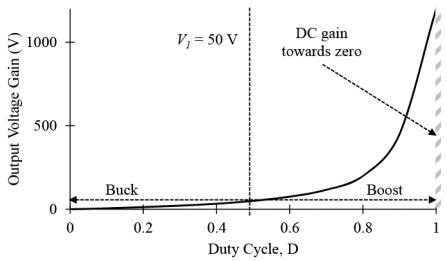

Fig. 6 *DC gain characteristics for the SEPIC structure*

the switch S. Thus, the returning current path flows through L_1 and L_2 and causes the circulating current to occur in both cycles.

Therefore, a modified bridgeless PFC SEPIC structure as shown in Fig. 5 is proposed to overcome the drawbacks of existing structure. The modified structure has several advantages such as a reduced number of power converter and switches, elimination of circulating current, and reduction of maximum current stress at line diodes and input capacitors. The parameters of the components are required to be optimised in order to minimise the THD_i and output voltage ripple, which inherently eliminate the dead zones as well as the additional energy at the output full bridge V_1. The principle of design parameters optimisation is based on the energy balance compensation between the input capacitor and output inductor. In addition, this structure of PFC converter is designed to operate in discontinuous conduction mode (DCM) with the merits of zero current turning on the power switch and zero current turning off in the output diodes. The THD_i is considered based on the stipulated standard such as International Electrotechnical Commission (IEC) 61000-3-2 that limits the harmonics produced by these devices for class D [30–32]. The pulse-width modulation (PWM) signal to the switch is generated by using the Altera DE2 as in [33, 34].

2 Modified single-switch bridgeless PFC SEPIC structure

This section discusses the fundamental principle, operating modes principle, design parameters of passive components, design parameters optimisation principle of bridgeless PFC SEPIC structure, and features of the modified structure.

2.1 Basic principle of SEPIC converter

Theoretically, when a duty cycle approaches unity, the DC gain reduces toward zero value [35]. The switching frequency needs to be considered for parameters optimisation purpose. On the occasion that the switching frequency increases, the ripple current of the inductor decreases. Fig. 6 shows the DC gain characteristics of the SEPIC converter. It is also known that the structure depicted in Figs. 1–5 consists of buck and boost operations, where for buck operation the duty cycle is <0.5 and for boost operation, the duty cycle is >0.5.

2.2 Operating modes principle of the modified single-switch bridgeless PFC SEPIC converter

The modified bridgeless PFC SEPIC structure circuit with a single switch is controlled by the duty cycle and timing waveform as shown in Fig. 7.

This circuit can be divided into ten operation modes and consists of positive-half and negative-half cycles. Fig. 8 shows the operation modes during the positive-half and negative-half cycles.

Mode-1 and Mode-6: Mode-1 is positive-half cycle, whereas Mode-6 is a negative-half cycle. When switch S is turned on, the energy is stored in L_1 at positive-half cycle and L_2 at negative-half cycle. At the same time, capacitors C_1 and C_2 are fully charged and inductor L_o stores energy from looping condition by the source. During this interval, capacitor C_o is discharged, diode D_o is turned off, and the power is supplied to the loads as shown in Figs. 7*a, b* and 8*a, b*.

Mode-2 and Mode-7: Mode-2 is positive-half cycle, whereas Mode-7 is a negative-half cycle. During the same state when the switch S is turned on, the inductors L_1 at positive-half cycle and L_2 at negative-half cycle store energy continuously from the input source. Meanwhile, the capacitors C_1 and C_2 are discharging through to the inductor L_o. During this interval, C_o is discharged, diode D_o is still in blocking mode and the power is supplied to the loads as shown in Figs. 7*a, b* and 8*c, d*.

Mode-3 and Mode-8: Mode-3 is positive-half cycle, whereas Mode-8 is a negative-half cycle. When the switch S is turned off, the inductors L_1 at positive-half cycle, L_2 at negative-half cycle,

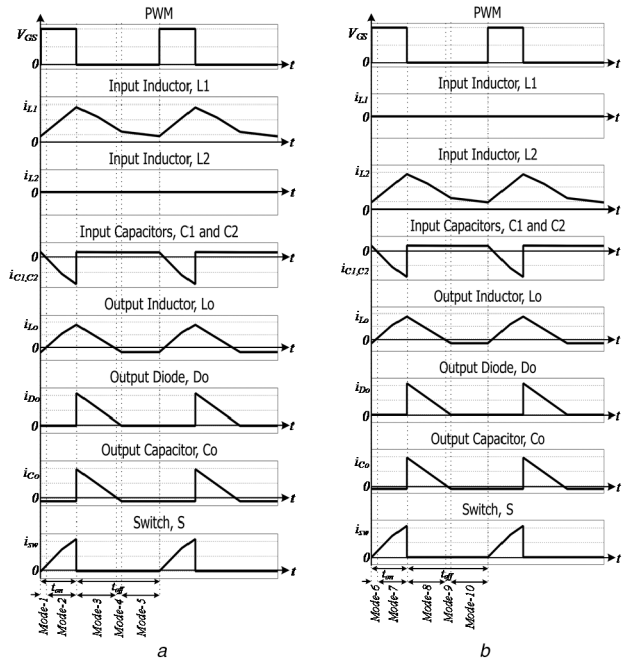

Fig. 7 *Key waveforms of the converter in Fig. 8 for*
(a) Positive-half cycle, ***(b)*** Negative-half cycle

and L_o are discharging. Meanwhile, the capacitors C_1, C_2, and C_o are charging through the freewheeling diodes D_o and the power is supplied to the loads as shown in Figs. 7*a, b* and 8*e, f*.

Mode-4 and Mode-9: Mode-4 is positive-half cycle, whereas Mode-9 is a negative-half cycle. During the same state when the switch S is turned off, the inductors L_1 at positive-half cycle and L_2 at negative-half cycle store energy to the capacitors C_1 and C_2. Meanwhile, the inductor L_o and capacitor C_o are discharging through the freewheeling diodes D_o and the power is supplied to the loads as shown in Figs. 7*a, b* and 8*e, f*.

Mode-5 and Mode-10: Mode-5 is positive-half cycle, whereas Mode-10 is a negative-half cycle. During the same state when switch S is turned off, the capacitors C_1, C_2, and inductor L_o store energy from looping condition by the inductors L_1 at positive-half cycle and L_2 at negative-half cycle. During this interval, capacitor C_o is discharging, diode D_o is turned off, and the power is supplied to the loads as shown in Figs. 7*a, b* and 8*c, d*.

2.3 Parameters design of modified single-switch bridgeless PFC SEPIC structure

Table 1 shows the specifications to design the passive elements, which are the capacitors and inductors. On the basis of the modes of operations, the values of passive elements are estimated based on the DCM condition [5, 29].

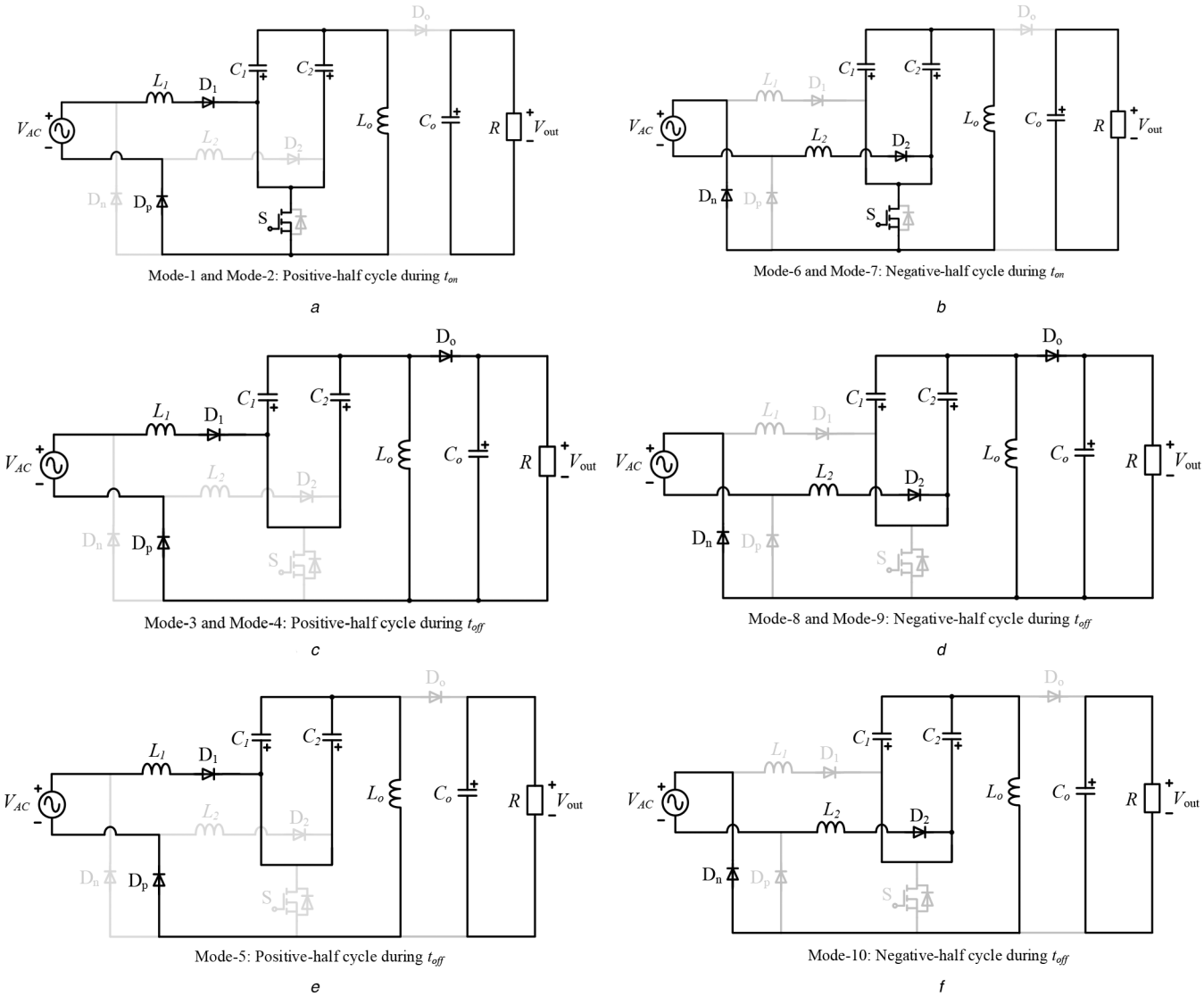

Fig. 8 *Modes of operations during positive-half and negative-half cycles*
(a) Mode-1 and Mode-2, ***(b)*** Mode-6 and Mode-7, ***(c)*** Mode-3 and Mode-4, ***(d)*** Mode-8 and Mode-9, ***(e)*** Mode-5, ***(f)*** Mode-10

Table 1 Specifications

Parameters	Values
input voltage, V_{AC}	50–100 V
frequency line, f_L	50 Hz
period of line voltage, T_L	0.02 s
output voltage (DC), V_o	48 V
output power, P_{out}	160 W
switching frequency, f_s	50 kHz
maximum input current ripple, Δi_{L1}	<25% of fundamental current
output voltage ripple, ΔV_o	<5% of V_o

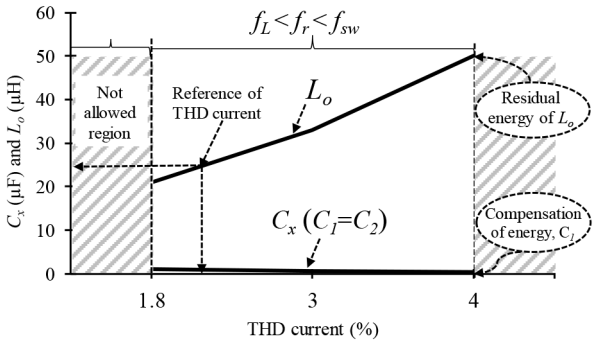

Fig. 9 *Design parameters optimisations of L_o and C_x with energy balance principle*

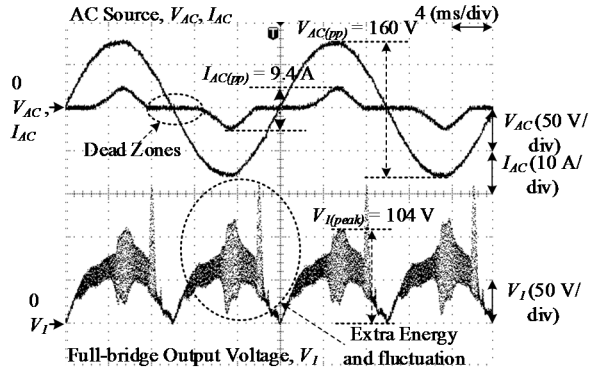

Fig. 10 *Dead zones occur at AC current source (refer to circuit structure in Fig. 2)*

2.3.1 Determination of input inductor: The input inductors (L_1 and L_2) are expressed in (1) with input voltage (V_{AC}) is in the positive-half and negative-half cycles

$$L_1 = L_2 = \frac{V_{AC}(t) \cdot D_1}{\Delta I_{Lx} \cdot f_s} \tag{1}$$

$$L_x = L_1 = L_2 \tag{2}$$

2.3.2 Determination of output inductor: The voltage conversion ratio M in terms of the rectifier parameter can be obtained by applying the power balance principle [30]

$$M = \frac{V_o}{\sqrt{2} \times V_{AC}} \tag{3}$$

The value of $K_{e-critical}$ can be evaluated from

$$K_e < K_{e-critical} = \frac{1}{2(M+2)^2} \tag{4}$$

To ensure the operation is in DCM, the following value of K_e is selected:

$$K_e = 0.85 \times K_{e-critical} \tag{5}$$

Thus, evaluating parameter K_e gives an equivalent inductance L_e value of

$$L_e = \frac{K_e \cdot R_L}{2 \cdot f_s} \tag{6}$$

The value of L_o can be expressed as follows:

$$L_o = \frac{2L_x \cdot L_e}{L_x - L_e} \tag{7}$$

2.3.3 Determination of input capacitor: The input capacitors C_1 and C_2 should not cause low-frequency oscillations with the converter inductors. Thus, the energy transfer of capacitors C_1 and C_2 are determined based on the inductors L_1, L_2, and L_o such that the line frequency (f_L) should be well below the switching frequency (f_s). Thus, a better initial approximation for choosing the resonant frequency (f_r) is given by [5]

$$f_L < f_r < f_s \tag{8}$$

$$f_r = \frac{1}{2\pi\sqrt{C_x(L_x + L_o)}} \tag{9}$$

$$C_x = C_1 = C_2 \tag{10}$$

2.3.4 Determination of output capacitor: The output voltage frequency ripple of the converter is two times of the input frequency. Therefore, C_o can be obtained as follows:

$$C_o = \frac{P_o}{4f_L \cdot V_o \cdot \Delta V_o} \tag{11}$$

2.4 Design parameters optimisation principle of the modified single-switch bridgeless PFC SEPIC structure

By referring to Fig. 2, the design parameters optimisation is applied to the conventional PFC SEPIC structure. Several conditions need to be considered as an ideal case to optimise the parameters of the passive components to ensure no additional energy occurs at the full-bridge output voltage V_1 and eliminate dead zones at the AC current source I_{AC}. Fig. 9 shows the graph of parameters optimisation of the input capacitor C_x and output inductor L_o versus the percentage of current THD. Formulae in (7) and (9) are used to optimise the design parameters of L_o and C_1. The selection of the design parameters is based on the energy balancing compensation between the input capacitor C_x and output inductor L_o. However, the allowable current THD range must be within 1.8–4% in order to estimate the capacitance of the capacitor C_x and inductance of the inductor L_o for optimisation purpose. The stored energies in C_x and L_o must be compensated with each other. Otherwise, the remaining energy of L_o will be transferred back to the source, and consequently affecting the quality of input line current and dead zones will exist as shown in Fig. 10. Besides, the residual energy can cause the additional energy to occur at full-bridge output voltage V_1 as shown in Fig. 10. The current THD of 2% is used as a reference to ensure the efficiency of the proposed converter is high and current THD is low, according to the IEC 61000-3-2 standard. On the other hand, this principle can be used for existing and modified single-switch bridgeless PFC SEPIC structures as shown in Figs. 4 and 5, respectively. Meanwhile, Fig. 11 shows the AC source and full-bridge output voltage after the design parameters optimisation is applied. The dead zones are inherently eliminated and the additional energy at the V_1 is minimised because the energy between C_1 and L_o compensates with each other with low-current THD.

On the occasion where the minimisation of the output voltage ripple is concerned, the capacitor current ripple Δi_c and capacitor voltage ripple ΔV_c are expressed by (12) and (13). In addition, the output voltage ripple is expressed by (15)

$$\Delta i_c = \Delta i_L = \frac{V_L}{L_o} D T_s \tag{12}$$

$$\Delta V_c = \frac{1}{C} \int i_c \, dt \tag{13}$$

$$\Delta V_{ESR} = \Delta i_c \cdot ESR \tag{14}$$

$$\Delta V_o = \Delta V_c \cdot \Delta i_{ESR} \tag{15}$$

On the basis of (11), the output voltage ripple reduces when the capacitance increases [36] and the output frequency is doubled from the line frequency for one cycle as shown in (15). The DC output depends on the full-wave and half-wave bridge rectifiers, as shown in Fig. 12

$$f_{line} = 2 \cdot f_{out} \tag{16}$$

After all the parameters are optimised by considering the availability of the components in the market, the modified single-switch bridgeless PFC SEPIC structure specifications are listed as shown in Table 2.

2.5 Features comparison of the modified and existing single-switch bridgeless PFC SEPIC structures

Comparison to the existing bridgeless PFC SEPIC structure [29] reveals that the modified bridgeless PFC SEPIC structure has the following distinctive features such as reduction of maximum current stress at the input capacitors and line diodes, undesired capacitive coupling loop, reduction of passive components, and elimination of circulating current, which increases the efficiency:

(i) Different from the existing structure presented in [29], the line diodes D_1 and D_2 are connected in series at the input inductors L_1 and L_2 and the slow-recovery diodes are needed for the line switching frequency which is $f_{line} = 50$ Hz. Hence, the high maximum current that occurs at the line diodes D_1 and D_2 can be reduced. Consequently, two fast-recovery diodes are not required in the modified bridgeless PFC SEPIC structure. Thus, a low-cost structure is obtained as well as improvement in the converter's efficiency.

(ii) Similar to the existing structure in [29], the input AC line voltage is always connected to the output ground through the slow-recovery diodes D_p and D_n. Therefore, the issue on high common-mode electromagnetic interference (EMI) emission can be resolved in the modified structure because the ground point is shared between the two diodes [37, 38].

(iii) By taking the positive-half cycle as a reference from the existing structure [29], during the whole positive-half line cycle, the metal–oxide–semiconductor field-effect transistor (MOSFET) S keeps turned on and turned off with a switching frequency of 50 kHz and with the input inductor L_1 in operation. When the MOSFET S is turned on, the current returns through the diode D_p and no current flows through the body diode of MOSFET S. During this interval, no looping current occurs at the input capacitors C_1 and C_2. Accordingly, when the MOSFET S is turned off, the current returns not only through the diode D_p but also through the input inductor L_2. In addition, the circulating current is also present because the input inductor coil of L_2 has low impedance at the low line frequency of 50 Hz as shown in Fig. 7. Hence, during the positive-half cycle, the inductance current i_{L2} is not zero. However, compared to the modified structure, when the MOSFET S is turned on and turned off, the current returns through the diode D_p and no current flows through to the body diode of MOSFET S and input inductor L_2. Thus, the circulating current is completely eliminated. However, the capacitive coupling loop current occurs at the input capacitors C_1 and C_2.

(iv) There is no current flow through the body diode of MOSFET S at low-frequency current during the turned on and turned off states. Thus, the selection of active switches between insulated gate bipolar transistor and MOSFET is to be made easier. This stems from the fact that the current returns only through the diodes D_p or D_n with no current flows through the body diode of inactive MOSFET S.

(v) On the occasion where the line diodes D_1 and D_2 are connected in series with the MOSFET S in [29], the input capacitors operates in different cycles which are C_1 during the positive-half cycle and C_2 during the negative-half cycle. Therefore, the reduction of the maximum current stress at the input capacitors C_1 and C_2 can be reduced with the operations of both cycles. According to (17) and (18), the capacitance increases when it is connected in parallel and the current flows through the input capacitors are divided into two paths. This resulted in the maximum current stress at the input capacitor to be reduced significantly

$$C_T = C_1 + C_2 \tag{17}$$

$$I_{CT} = I_{C1} + I_{C2} \tag{18}$$

Nevertheless, the modified structure can be improved by reducing the input capacitance by using a single input capacitor to ensure the undesired capacitive coupling loop no longer exists, the circulating

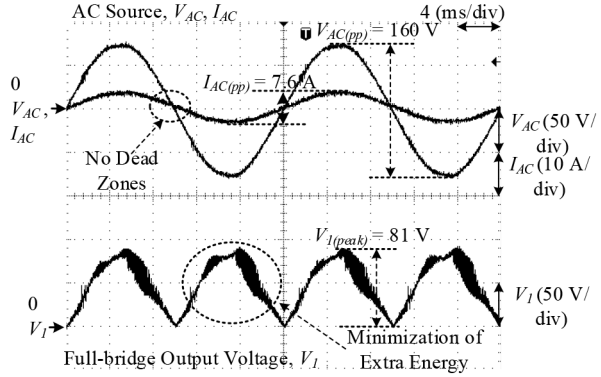

Fig. 11 *Extra energy occurs at full-bridge output voltage V_1 (refer to circuit structure in Fig. 2)*

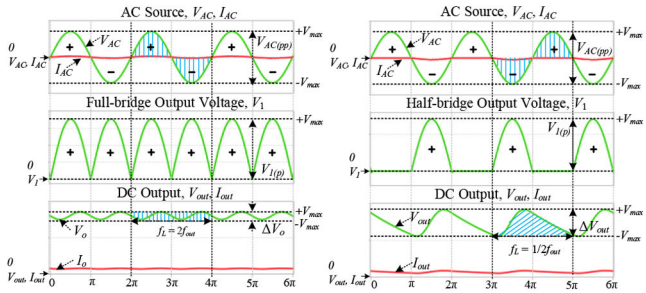

Fig. 12 *DC output for full-bridge and half-bridge rectifiers (refer to circuit structure in Fig. 2)*

Table 2 Design parameters optimisation of passive elements

Parameters	Values
input inductors, L_x ($L_1 = L_2$)	2.2 mH
output Inductor, L_o	22 μH
input capacitors, C_x ($C_1 = C_2$)	1 μF
output capacitor, C_o	3300 μF

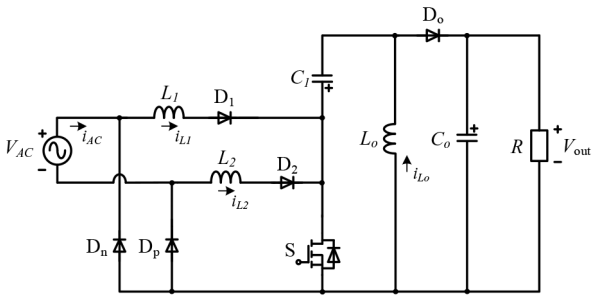

Fig. 13 *Improved modified single-switch bridgeless PFC SEPIC structure*

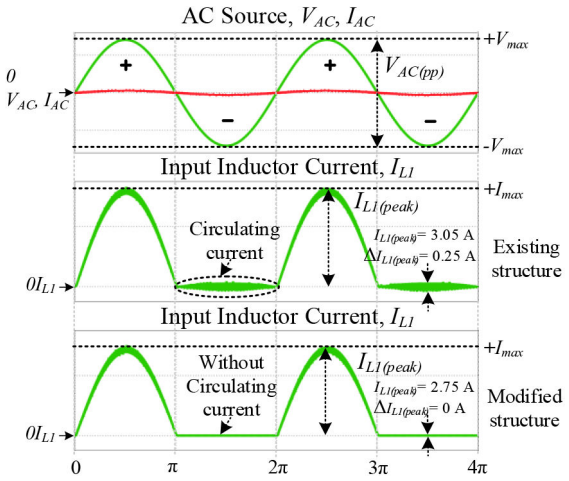

Fig. 14 *Current at input inductor L_1 for the existing structure and modified structure obtained from simulation*

current is eliminated, and the low-side current sensing noise is reduced as shown in Fig. 13.

3 Simulation results

The modified single-switch bridgeless PFC SEPIC structure is simulated by using Plexim software with the specification and parameters as shown in Tables 1 and 2. Fig. 14 shows the AC voltage source and AC current source in-phase for the modified structure. During positive-half cycle, the existing structure shows the occurrence of circulating current with the inductor current ripple of 0.25 A during the negative-half cycle. On the other hand, the same type of current for the modified structure is 0 A. Besides, the peak current of L_1 for the existing structure is 3.05 A while the peak current of L_1 for the modified structure is slightly reduced to 2.75 A. From the observation, during negative-half cycle, the inductor current ripple at L_1 is the same as the current during positive-half cycle at peak time. The inductor current ripple at L_1 receives energy from the AC source during negative-half cycle. Hence, the L_1 is forced to operate during negative-half cycle due to the energy buffer from the AC source. For that reason, the energy buffer during negative-half cycle is also known as the circulating current.

4 Experimental results

The experimental results are discussed by referring to Tables 1 and 2, which focus on the minimisation of current THD and output voltage ripple, elimination of circulating current losses, reduction of maximum current stress at the input capacitors C_1 and C_2, and reduction of maximum current stress at the line diodes D_1 and D_2. The experimental results are confirmed and agreed with the design parameters. Fig. 15 shows the experimental setup of the proposed converter.

4.1 Minimisation of current THD

Fig. 16 shows the current THD of the AC source by using the output inductor $L_o = 2.2$ mH before the optimisation and $L_o = 22$

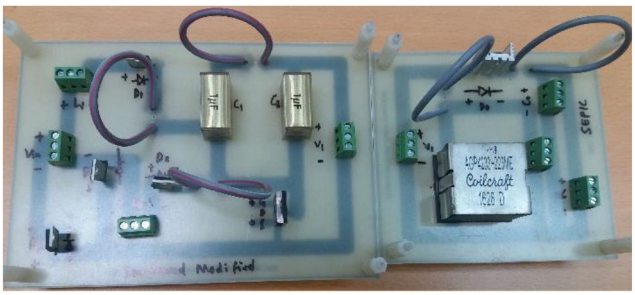

Fig. 15 *Experimental setup of the proposed converter*

μH after the optimisation with a fixed output capacitance of 3300 μF. Fig. 16*a* shows the AC current source contains a single harmonic distortion caused by the unbalanced energy compensation between the input capacitors and output inductor. Therefore, the AC current source is not a pure sinusoidal wave as the AC voltage source is used and the occurrences of dead zones. The AC current source of peak-to-peak is 9.4 A and AC voltage source of peak-to-peak is 160 V. The output current ripple is 0.18 A and the output voltage ripple is 9 V. However, these results do not imply that this modified structure could not meet the IEC 61000-3-2 standard. The optimised parameters are also considered to ensure the harmonics limit is always within the range stipulated by the IEC 61000-3-2 standard, where the THD_i must be <5%. Fig. 16*b* shows the pure sinewave of the AC current source, which is similar as the AC voltage source waveform with the AC current source of peak-to-peak, is 7 A and AC voltage source of peak-to-peak is 160 V. On the basis of the optimised parameters, the energy between the input capacitors and output inductor is balanced, and the dead zones are inherently eliminated. The output current ripple is 0.16 A and the output voltage ripple is 7 V.

The value of current THD is measured by using power analyser, and all data are tabulated in a single graph. Also, a fixed switching frequency of 50 kHz and output capacitance of 3300 μF for both output inductors are used to observe the current THD in terms of the input current ripple. From Fig. 17*a*, the current THD of the L_o

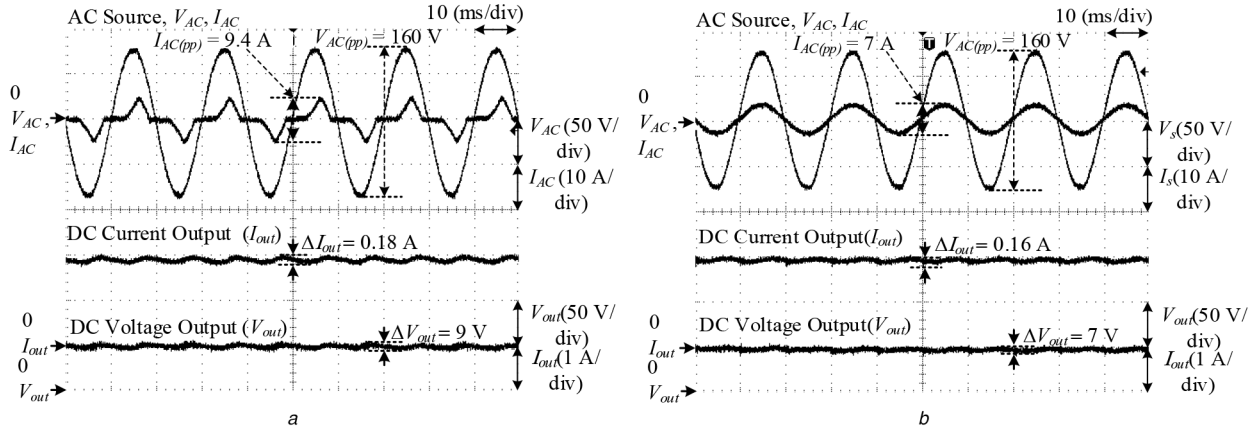

Fig. 16 *Current THD of input source (refer to circuit structure in Fig. 2)*
(a) 2.2 mH, ***(b)*** 22 µH

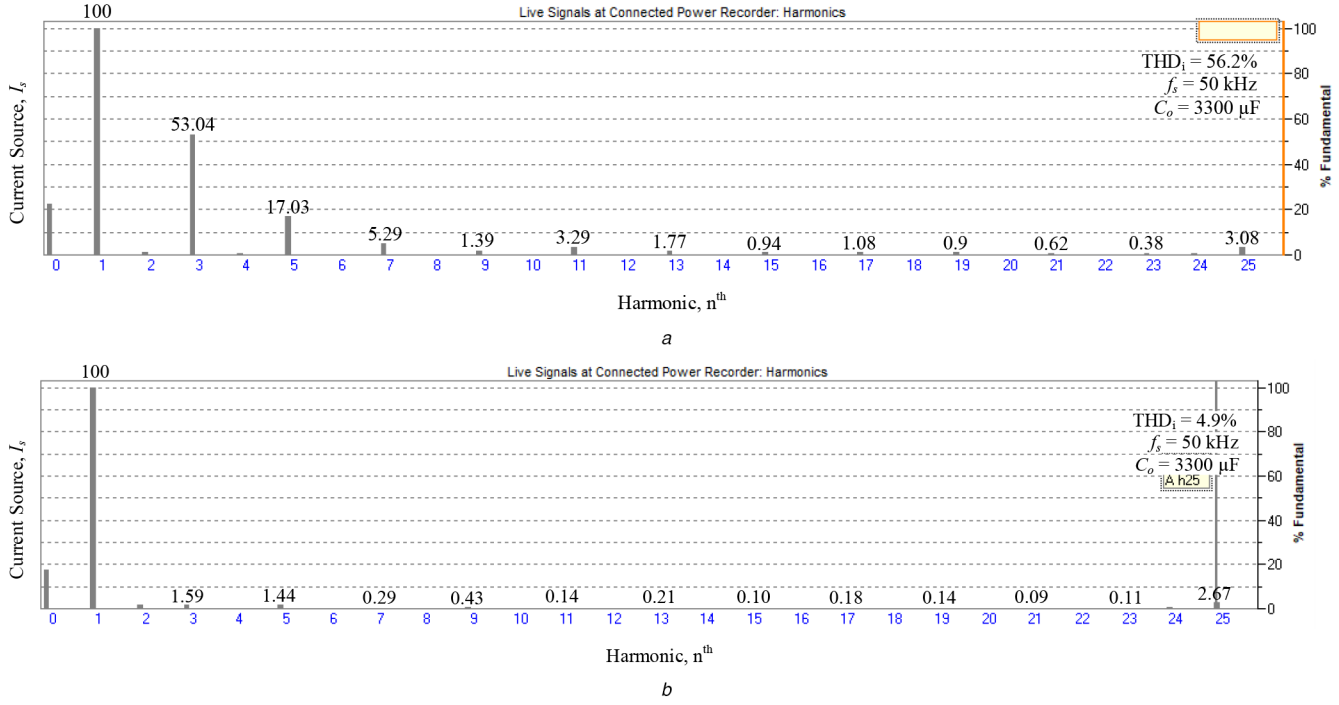

Fig. 17 *Current THD component (refer to circuit structure in Fig. 5)*
(a) 2.2 mH, ***(b)*** 22 µH

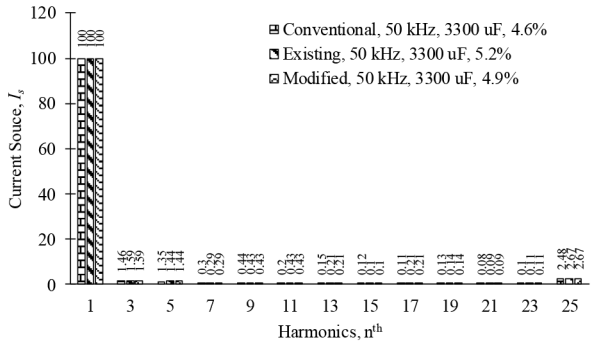

Fig. 18 *Frequency spectrum with various frequencies and output capacitor*

= 2.2 mH is used, and the result shows a high ripple current at the AC current source with THD_i = 56.2%. It is also observed that the result does not meet the IEC 61000-3-2 standard from the poor current THD, where the 3rd and 5th highest harmonics foresee the need to be supressed as low as possible. Thus, Fig. 17*b* shows the current THD of L_o = 22 µH is following the IEC 61000-3-2 standard with THD_i = 4.9% which is the result of minimisation of the 3rd and 5th harmonics component.

The data of each harmonic component for the three structures, i.e.: conventional, existing, and modified, are shown in Fig. 18. The results demonstrate that the conventional and modified structure can achieve the IEC 61000-3-2 standard, where the THD_i for the former is 4.6% and THD_i for the latter is 4.9%, as compared with the existing structure where the THD_i is 5.2%, which does not meet the requirement of IEC 61000-3-2 standard.

4.2 Minimisation of output voltage ripple

Fig. 19 shows the comparison of output voltage ripple when the output capacitances used are 470 and 3300 µF with a fixed switching frequency of 50 kHz and output inductance of 22 µH. It can be seen that the output voltage ripple is reduced from 19 to 7 V when the output capacitance is increased. However, the output current ripple also decreases from 0.58 to 0.14 A when the capacitance is increased. Fig. 19*a* shows the output voltage ripple is 19 V and the output current ripple is 0.58 A with the output capacitance of 470 µF. The AC current source of peak-to-peak is 7 A and AC voltage source of peak-to-peak is 160 V. The DC output is not sufficiently smooth because the output capacitance is not large enough to filter the output voltage. On the occasion where the

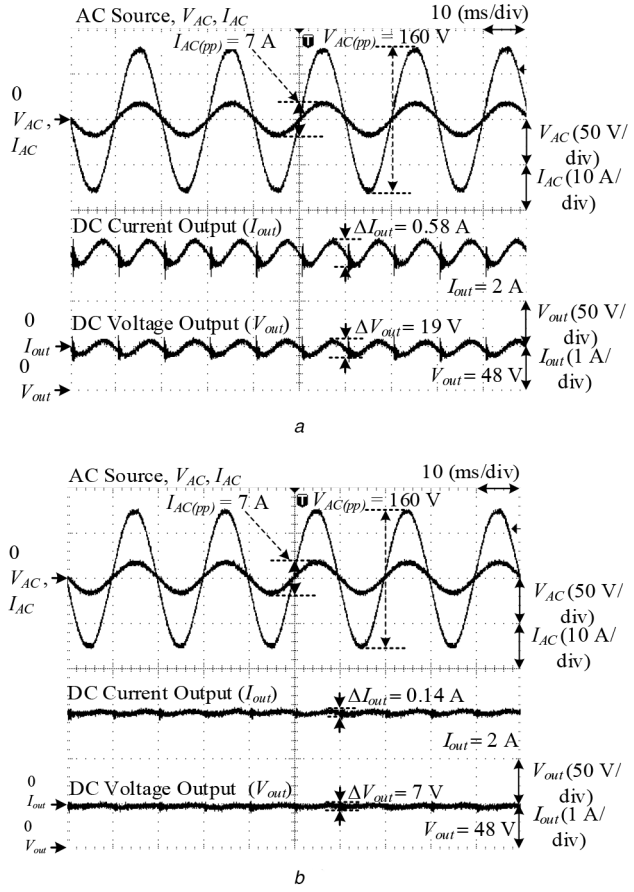

Fig. 19 *Output voltage ripple with output capacitance (refer to circuit structure in Fig. 5)*
(a) 470 μF, ***(b)*** 3300 μF

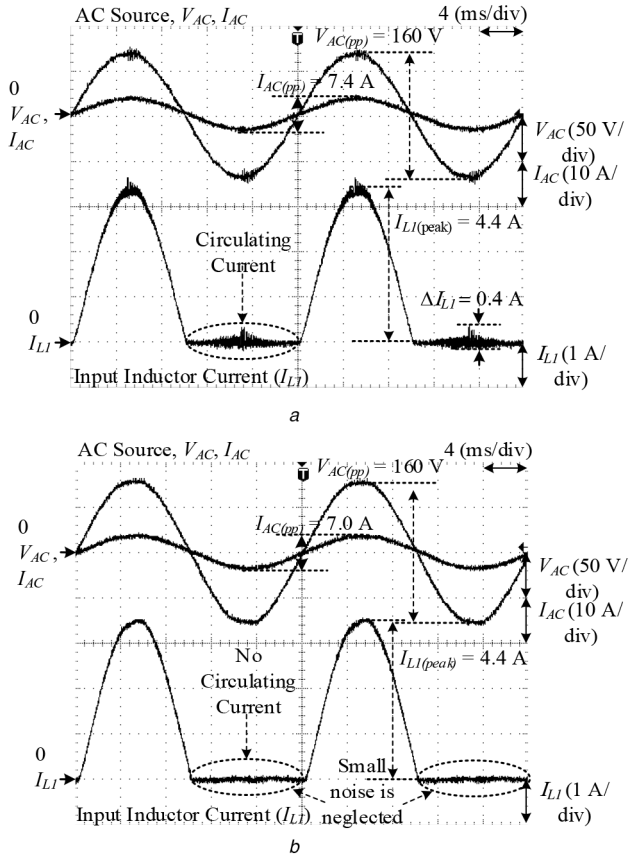

Fig. 20 *Elimination of circulating current*
(a) Existing structure (Fig. 4), ***(b)*** Modified structure (Fig. 5)

output capacitance is 3300 μF, the output voltage ripple is reduced to 7 V and the output current ripple is 0.14 A. This is because when the capacitance is high, the output voltage ripple is reduced. Thus, the function of the output capacitor is to smooth out the voltage as shown in Fig. 19*b*. The AC current source of peak-to-peak is 7 A and the AC voltage source of peak-to-peak is 160 V. It can be seen that the experimental results approximately agree with the theoretical analysis as and when the capacitance increases, the output voltage ripple decreases. The spike of the output voltage waveform depends on the parasitic element parameters and the difference in the output voltage ripple waveforms will cause various effects when different types of capacitors are used. Besides, it is confirmed that the theoretical part in Section 2.4 is verified. Thus, it can be observed that the theoretical analysis, simulation, and experimental results agree well with each other.

4.3 Elimination of circulating current

Fig. 20 illustrates the experimental results for both structures, i.e. existing structure and modified structure. All parameters are the same as mentioned in Tables 1 and 2.

The waveform shows that in the proposed converter, after breaking the undesired capacitive coupling loop, the circulating current is minimised, which match very well with the theoretical analysis in Section 2.5. Fig. 20*a* shows the result of existing structure which consists of circulating current at the input inductors L_1 and L_2 for both cycles. It can be seen that, when the input inductor L_1 operates in positive-half cycle, the peak current of the input inductor $I_{\mathrm{L1(peak)}}$ is 4.4 A. Meanwhile, during the negative-half cycle, the circulating current is 0.4 A with the AC current source of peak-to-peak is 7.4 A and AC voltage source of peak-to-peak is 160 V.

Compared to Fig. 20*b*, the circulating current is 0.1 A and small noise is neglected. The input inductor $I_{\mathrm{L1(peak)}}$ is 4.4 A which is the same as the existing structure. The AC current source of peak-to-peak is 7.0 A and the AC voltage source of peak-to-peak is 160 V. The experimental verification shows that the modified structure can eliminate the circulating current significantly.

4.4 Reduction of maximum current stressed at input capacitors C_1 and C_2

Fig. 21 illustrates the experimental verification of the existing and modified structures to reduce the maximum current stress at the input capacitors C_1 and C_2.

By considering the positive-half cycle, Fig. 21*a* shows that capacitor C_1 operates only in the positive-half cycle. The peak current of the input capacitor $I_{\mathrm{C1(peak)}}$ is 10.5 A, where the AC current source of peak-to-peak is 7.4 A and the AC voltage source of peak-to-peak is 160 V. The undesired capacitive coupling loop no longer exists between C_1 and C_2, where previously the maximum current stress at input capacitors is high because it operates only during the half cycle.

On the other hand, when comparing with Fig. 21*b*, the peak current of the input capacitor $I_{\mathrm{C1(peak)}}$ is 4.8 A, where the AC current source of peak-to-peak is 7.0 A and AC voltage source of peak-to-peak is 160 V. Capacitor C_1 operates in both cycles, and hence reduces the maximum current stress at the input capacitors. However, the undesired capacitive coupling loop exists between C_1 and C_2 and the input capacitor can be reduced to one. The results of both structures are confirmed with the theoretical analysis as discussed in Section 2.5.

4.5 Reduction of maximum current stress at line diodes D_1 and D_2

Similarly, in Section 4.4, the maximum current stresses at the line diodes D_1 and D_2 can be reduced significantly by replacing the line diodes at the input inductors L_1 and L_2, where the line frequency is 50 Hz. Fig. 22 illustrates the experimental verification of the existing and modified structures to reduce the maximum current

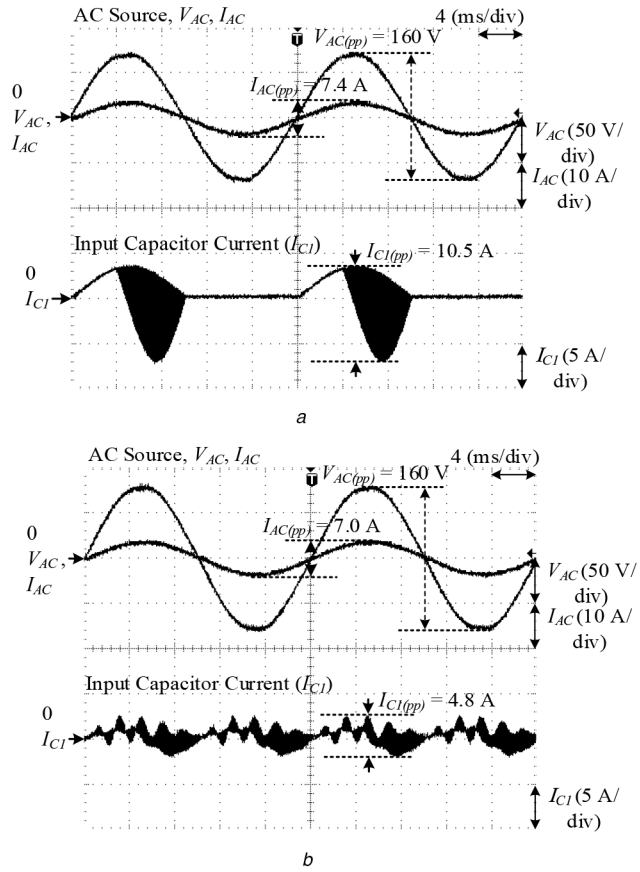

Fig. 21 *Reduction of maximum current stressed at input capacitors*
(a) Existing structure (Fig. 4), ***(b)*** Modified structure (Fig. 5)

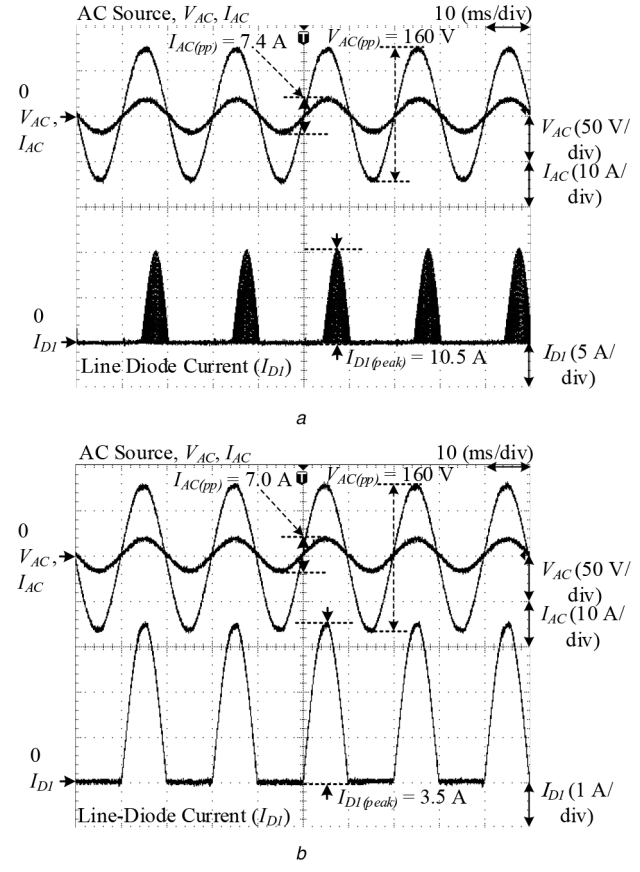

Fig. 22 *Reduction of maximum current stress at line diodes*
(a) Existing structure (Fig. 4), ***(b)*** Modified structure (refer to circuit structure in Fig. 5)

stress at the line diodes D_1 and D_2. By considering only half cycle, Fig. 22*a* shows that the D_1 operates only in the positive-half cycle. The peak current of the line diode $I_{D1(peak)}$ is 10.5 A, where the AC current source of peak-to-peak is 7.4 A and AC voltage source of peak-to-peak is 160 V. The maximum current stresses at the C_1 and D_1 is similar because the positions of the components are in series with the MOSFET *S*. Therefore, the current flows through the C_1 and D_1 are high without the capacitive coupling loop because of the switching frequency of 50 kHz. By comparing with Fig. 22*b*, the peak current of the line diode $I_{D1(peak)}$ is 3.8 A, where the AC current source of peak-to-peak is 7.0 A and AC voltage source of peak-to-peak is 160 V. The maximum current stresses at C_1 and D_1 are not identical because the frequencies of both components are different as f_{line} is 50 Hz, whereby f_{sw} is 50 kHz. However, the maximum current stresses at C_1 and D_1 reduce significantly with the capacitive coupling loop.

5 Conclusion

In this paper, a modified bridgeless PFC SEPIC converter has been proposed and experimentally verified. The experimental results have shown a good agreement with the designed results. The current THD is 4.9% and less than the previous parameters optimisation. The requirement of IEC 61000-3-2 standard has been achieved by balancing the energy compensation of the passive elements. Moreover, the circulating current losses and dead zones have been eliminated with the output frequency doubled in value from the line frequency. Other than that, with higher PF and efficiency, the structure can be applied to most of consumer electronic products with 160 W rating in the market. This topology uses the bridgeless SEPIC structure with a single switch (MOSFET). A high PF can be achieved by applying any PWM switching patterns.

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